

Control Principles and On-Chip Circuits for Active Cooling Using Integrated Superlattice-Based Thin-Film Thermoelectric Devices

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Abstract—Superlattice thin-film thermoelectric coolers (TECs) are emerging as a promising technology for hot spot mitigation in microprocessors. This paper studies the prospect of on-demand cooling with advanced TECs integrated at the back of the heat spreader inside a package (integrated TEC). Using thermal compact models of the chip and package with integrated TECs, the control principles for TEC-assisted transient cooling are presented. The control principles are implemented in a 130-nm CMOS process and cosimulated with the thermal system to show their feasibility and energy overheads. The simulation results show potential for extending the time for which a chip and package can sustain a high power load.

Index Terms—Active cooling, cosimulation, hot spot, TEC control, thermoelectric coolers (TECs).

I. INTRODUCTION

LOCALIZED high heat fluxes within a chip result in localized high-temperature regions or hot spots. The hot spot determines the maximum chip temperature and can set the limit on the maximum allowable power, referred to as the thermal design power (TDP), of a microprocessor chip or package [1]–[5]. The conventional cooling methods using a heat sink and air flow aim to reduce average temperature of the chip. Reducing hot spot temperature with air cooling requires a very high flow rate leading to high cooling power and reduced system efficiency [1]–[3]. Because of the time-varying nature of the power dissipation, additional localized cooling can be provided only when hot spots appear the maximum temperature can be reduced. This is referred to as on-demand cooling.

Dynamic thermal management (DTM) mechanisms like throttling, voltage-frequency-scaling, or thread/activity migration are currently invoked when the chip temperature reaches

a certain threshold level to control overheating, but DTM results in appreciable energy/performance overheads. Further, techniques like turbo-boosting [6] and “computational sprinting” [5] that intentionally increase operating frequency/power over the nominal limit for critical processes are becoming popular for performance enhancements. If higher power events can be sustained over longer time duration without violating temperature constraints and invoking DTM, the system performance can be improved. Hence, there is a pressing concern for transient thermal management, both at the architectural and packaging levels. On-demand active cooling is a strong candidate for future packages, as it could provide the ability to sustain higher transient power, leading to extended performance.

Recent advances in superlattice Bi₂Te₃-based thin-film thermoelectric coolers (TECs) have shown significant promise in the on-demand cooling of hot spots. The TEC operates on the basis of the Peltier effect by dumping heat from its hot side to its cold side when a current flows through it [1]. The amount of heat taken away is proportional to the difference in the temperature and current through the TEC. The high figure of merit (ZT) of these thin-film superlattices and their high heat-flux pumping capability make them very attractive material for use in electronic devices. ZT is defined as a dimensionless unit that is used to compare thermoelectric materials. $ZT = S^2\sigma T/\kappa$, where S is the Seebeck coefficient, T is the absolute temperature, and σ and κ are the electrical and thermal conductivities, respectively. The higher the ZT the better the material is said to be when used as a TEC. Experimentally, integration of TECs with the thermal interface material (TIM) in a processor package has been demonstrated with total hot spot cooling of up to 15 °C [1]. Further, as cooling is controlled by an electrical current, the TEC provides the opportunity for on-demand run-time control of this additional cooling [1], [7]–[9].

This paper studies the feasibility of on-demand cooling using integrated superlattice thin-film TECs (Fig. 1). This paper presents a compact model of the electrothermal behavior of the superlattice thin-film TEC integrated within a package (Fig. 1). The full-chip model is used to develop control principles to manage transient temperature variations of an IC using TEC-assisted on-demand cooling. The proposed controllers are designed in a commercial 130-nm CMOS process and

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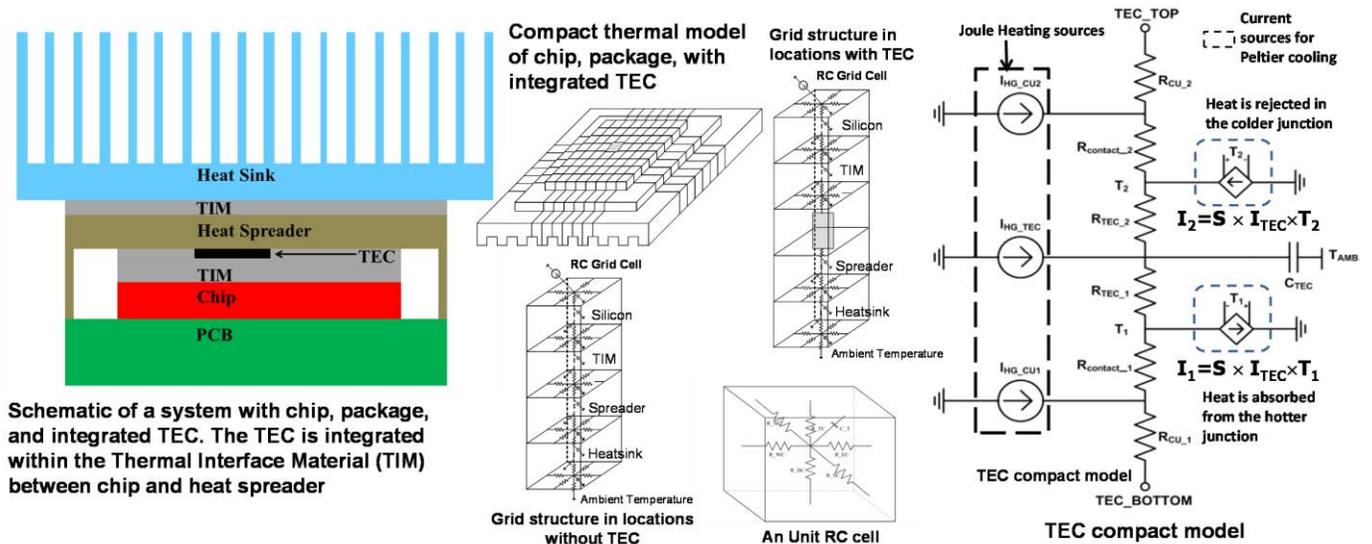


Fig. 1. System schematic and the compact thermal model of the chip, package, and integrated TEC. Compact thermal model is based on distributed RC network for the chip and package. Circuit compatible SPICE level compact model of the TEC includes R, C, and voltage controlled current sources to represent Peltier cooling and Joule heating. The model captures both transient and steady-state TEC behavior.

integrated with the thermal package model. Electrothermal cosimulations are performed to characterize the thermal behavior of the chip with the integrated TEC and controller. The simulation results show that TECs can help sustain a higher power load in a processor for a longer duration without causing thermal violations. The energy overhead associated with the control principles is discussed.

The rest of this paper is organized as follows. Section II presents related work and the contributions that this paper makes; Section III presents the modeling methods; Section IV discusses the effectiveness of steady-state and transient cooling; Section V discusses high-level control principles and the design of the controllers in CMOS; Section VI presents the analysis of the controllers and further discussion; and Section VI summarizes this paper.

II. RELATED WORKS

The material innovation for improving ZT and modeling of superlattice TECs has been the subject of much recent research [1], [9]–[11]. Detailed SPICE models have been presented in [12] and [13], but these models only model the thermoelectric material and do not include the contact resistance effects and integration within a full package.

Limited full-chip analysis of the integration of TECs in a system has been performed. Long *et al.* have explored algorithms for optimal placements of TECs in a chip to maximize the cooling efficiency when they are active [16], [17]. While the developed method helps in optimal TEC placements, it fails to consider the transient analysis of TECs and chip temperature. Chaparro *et al.* [18] have performed system-level trace-driven architectural studies to understand the effects of TEC integration within a microprocessor [19]. The authors have performed trace tests in three different configurations, focusing on an extreme performance, ED²-oriented, and a TDP-constrained case. The extreme performance scenario

shows the most promise. Although this paper does an excellent job at analyzing the TEC power overhead and execution time gains in a real workload, it does not describe the TEC model in detail or consider the transient behavior of the TEC.

Compared with the prior works, this paper makes the following contributions. First, the thermal compact models presented in this paper consider the 3-D distributed thermal system model of the TEC and full package. The developed compact models allow for accurate and fast analysis of the TEC and package characteristics. Second, this paper analyzes the implications of using TECs for transient thermal management, instead of facilitating steady-state cooling. Finally, for the first time, this paper integrates the thermal compact models of the TEC and chip/package with the circuit level representation of the TEC controller designed in a 130-nm CMOS technology to perform accurate electrothermal simulation. The integrated electrothermal simulation focuses on the transient behavior of the TEC and studies the impact on the transient temperature pattern. The analysis clearly shows the control energy/performance implications of different circuit design decisions and proves the feasibility of TEC-assisted cooling with on-chip controller.

III. MODELING METHODOLOGY AND VALIDATION

Fig. 1 shows the geometry of the chip, package, and integrated TEC. The TEC is embedded within the TIM and in contact with the heat spreader.

A. Thermal Model for Chip and Package

The well-known analog relationship between thermal and electrical properties is used to perform thermal simulations using SPICE [20]. More specifically resistors model material conductance, capacitors model specific heat, electrical current represents heat flux, and the voltage at a given node represents the absolute temperature. Fig. 1 shows the 3-D distributed

RC-based thermal model for the system. The materials are assumed to be isotropic in all directions. The resistances and capacitances of the unit cell are estimated based on the grid size [i.e., the thickness (L) and the cross-sectional area (A) of unit cell] and the material properties [the thermal conductivity (κ), the density (ρ), and the specific heat (c_p)] as follows:

$$R_{\text{cond}} = \frac{L}{\kappa A} \text{ and } C = \rho c_p. \quad (1)$$

B. Compact Thermal Model for TEC

The TEC operates on the basis of the Peltier effect by dumping heat from the hot side to the cold side when a current flows through it. The amount of heat taken away is proportional to the difference in the temperature as well as the current through the TEC. There is also Joule heating (I^2R) within the TEC that can potentially exceed the Peltier cooling at high current. However, the Peltier effect occurs on the surface of the TEC, and hence occurs on shorter time scales than Joule heating, which is uniform across the entire TEC [21]. The compact model shown in Fig. 1 is developed to capture the aforementioned effects. The Peltier cooling of the TEC device was incorporated by adding heat (proportional to SIT_1) at the hot side and subtracting heat (proportional to SIT_2) from the cold side of the superlattice, where T_1 and T_2 are the temperatures of the hot and cold sides, respectively. There are heat generation (HG) sources that model I^2R losses in the TEC as well as the Cu contacts. There are contact resistances representing the parasitic resistances between the Cu and TEC superlattice. The capacitor is lumped and placed in the middle of the TEC. The addition of the capacitor is an improvement in [16]–[18] as it allows for the modeling of the specific heat and hence, the transient behavior of the TEC.

C. Model Validation

A full chip with size $9 \text{ mm} \times 9 \text{ mm}$ with a single $3 \text{ mm} \times 3 \text{ mm}$ TEC device at the center is used for system analysis. The TEC is $100\text{-}\mu\text{m}$ thick and has an $8\text{-}\mu\text{m}$ -thick superlattice material sandwiched between two metallic layers of contacts. The TEC is made of 7×7 grid of n-p couples of p-type $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ and n-type $\text{Bi}_2\text{Te}_3/\text{Bi}_2\text{Te}_{2.83}\text{Se}_{0.17}$. The electrical/thermal contact resistances at the interface of the superlattice-metal layer ($10^{-11}\Omega\text{m}^2$; $10^{-6} \text{ m}^2\text{K/W}$) and at the interface of the TEC device–heat spreader layer ($10^{-10}\Omega\text{m}^2$; $8 \times 10^{-6} \text{ m}^2\text{K/W}$) are taken from [1]. The value of S is considered to be $300 \mu\text{V/K}$ based on experimental measurements in [1]. The heat sink was modeled using a constant convection with a heat transfer coefficient (HTC) and hence an equivalent resistance to the ambient temperature. Equations for efficiency of straight rectangular fins [22] modeled the extra spreading that occurred near the edges where the heat spreader ($23 \text{ mm} \times 23 \text{ mm}$) extended over the chip. The TEC and full package models were verified against a finite volume element analysis with FLUENT [8], [14] and demonstrated very good accuracy (Fig. 2, simulations with $\text{HTC} = 2500 \text{ W/m}^2\text{K}$). The FLUENT-based TEC model is validated against the measured results in [1]. The detailed model validation has been thoroughly reported in [14] and [15].

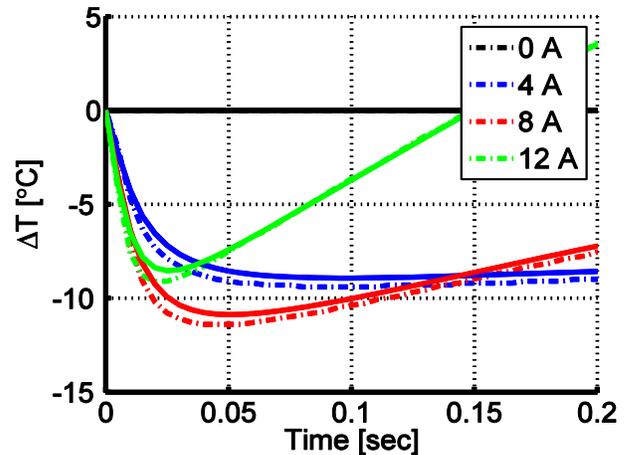


Fig. 2. Validation of the TEC model with integrated chip/package model showing accuracy of the transient behavior of the integrated chip, package, and TEC. Solid curves: FLUENT model. Dashed curves: compact model.

IV. TEC-ASSISTED COOLING

A. TEC-Assisted Steady-State (DC) Cooling

We first study the feasibility of “DC” cooling. Fig. 3(a) shows the steady-state silicon temperature at the location beneath the TEC as the total chip power is increasing and the TEC is always turned ON. For a target chip temperature, we observe that increasing the TEC current initially allows more power to be dissipated in the chip. For instance, for a target operating temperature of $60 \text{ }^\circ\text{C}$, a 3-A current through the TEC allows $\sim 12\%$ additional chip power compared with having no current ($I = 0$) in the TEC. The extra power can be exploited to increase steady-state performance (e.g., higher clock frequency) for a given package. However, Fig. 3(a) suggests that the overall improvement is expected to be marginal. Further increase in the TEC current introduces high Joule heating and the chip reaches a higher steady-state temperature for same power.

B. TEC-Assisted Transient Cooling and System Performance

We next study the implications of TEC-assisted cooling when the chip receives a large power spike [Fig. 3(b)]. It is important to note that even adding a TEC without any current flowing through it (i.e., $I = 0 \text{ A}$) is beneficial compared with the no TEC [package only in Fig. 3(c)] case, as the TEC’s copper contacts provide better heat conduction than the TIM material [Fig. 3(c), simulations with $\text{HTC} = 2500 \text{ W/m}^2\text{K}$]. With a finite TEC current ($I = 3 \text{ A}$), we can see an initial dip in the temperature when the TEC turns ON. After a interval, the temperature starts rising again and ultimately reaches a lower steady-state temperature compared with the case with no TEC current ($I = 0$). The initial temperature drop is because the Peltier cooling starts operating immediately after the TEC is turned ON, while the response time for the Joule heating is marginally higher. When the Joule heating becomes significant, the temperature starts rising at a faster rate. As the current is increased further (3–6 A), we see a greater initial cooling, but the rate of increase after the initial dip is much higher and hence the temperature becomes higher than the 3 A case. The transient cooling obtained with the

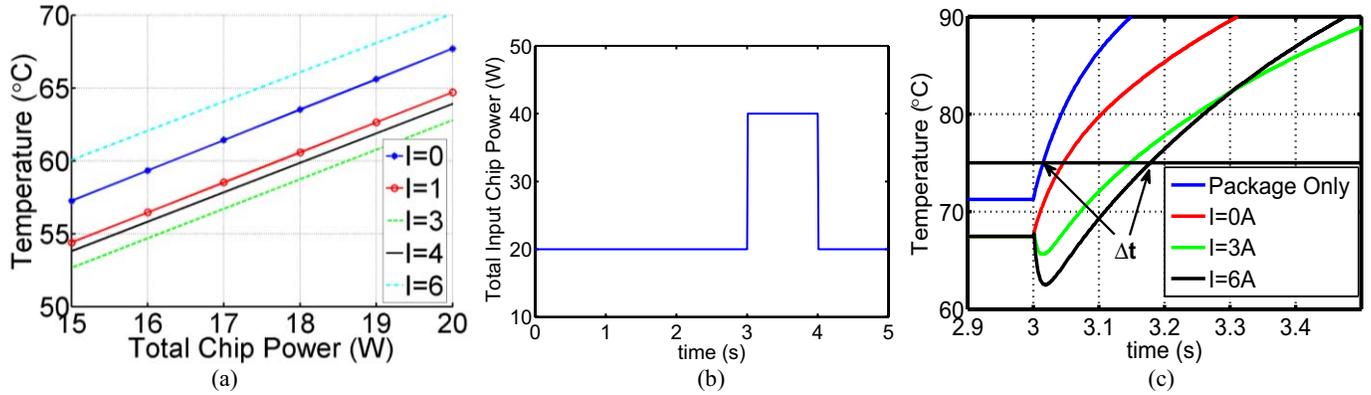


Fig. 3. TEC-assisted cooling. (a) DC cooling and steady-state temperature directly under the TEC. (b) Transient power pulse applied to the chip modeling a heavy workload. (c) Transient response of chip and package with 1 s power pulse applied. The concept of workload extension is shown. We can see a having a TEC current can significantly increase the time required to reach a target temperature (t of 150 ms). This is very significant in reducing the performance and power overheads associated with DTM in microprocessor.

TEC can significantly reduce the rate of increase of the chip temperature and hence, can sustain a power pulse for longer duration without violating thermal constraints. For example, Fig. 3(c) shows that a TEC current of 6 A can allow the system to remain under a target temperature of 75 °C for an extended time (Δt in the order of 100 ms) period.

V. CONTROLLER FOR ON-DEMAND TEC-ASSISTED COOLING

In this section, we present the principles for efficient control of TECs to exploit their potential in managing transient temperature. This is a control problem of reducing the thermal events (i.e., sustain a power pulse for a longer period) before the chip temperature crosses a threshold and the need to invoke DTM arises. The control principles are based on sensing the temperature to activate or deactivate the TECs. Turning the TEC off reduces the energy dissipated in the TEC. Advanced on-chip temperature sensors have submillisecond sampling time and less than 0.5 °C resolution [23], [24], justifying the feasibility of fine-grain control of the TEC activation/deactivation.

We first consider a threshold-based controller (ThBC) where sensed temperature is compared with a threshold. The TEC is turned on when the temperature crosses a certain threshold and it is turned off when temperature is less than the threshold. The controller aims to regulate the temperature near the threshold and delays the occurrence of the thermal event. However, the TEC suffers from continuous ON/OFF transitions (limited by the sampling frequency of the sensor) that could lead to degraded TEC reliability.

We explore an alternative approach, referred to as the maximum cooling-based controller Maximum Cooling Based Controller (MCBC), to minimize the number of transitions. Here we turn the TEC on beyond a threshold temperature but allow the temperature to reach its minimum value before turning the TEC OFF. This helps exploit the initial high transient cooling offered by the TECs [see Figs. 2 and 3(c)]. However, the Joule heating starts causing additional heating past the minimum point. Hence, the control principle is to turn the TEC on when the threshold temperature is reached,

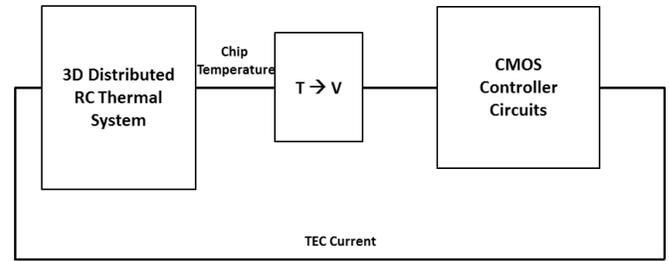


Fig. 4. Electrothermal cosimulation framework.

turn it OFF after the minima is reached, and turn it back ON when temperature crosses the threshold again.

The circuit level designs and simulations of the ThBC and MCBC controllers are performed in 130-nm CMOS technology. A circuit level model of the temperature sensor was used as discussed later. The electrical model of the TEC used in the simulation framework was a simple Thevenin equivalent resistance. The electrical resistance of the TEC is the only parameter that defines the current flowing through the TEC and will dictate the size of power FET that is required on chip. The equivalent electrical resistance for the TEC was based on the experimental results in [1] and the TEC size as defined in our thermal simulation framework [14], [15]. The total electrical resistance of the TEC and Cu contacts used for the simulations was 113 m Ω .

The controllers are integrated with the compact thermal model of the system, shown in Fig. 1(b), to perform electrothermal cosimulation (Fig. 4). The electrothermal cosimulation helps accurately characterize the effect of the TEC control on transient temperature considering the electrical response time of the sensors and controllers as well as energy overhead. The complexity of the transistor-level model of the CMOS controller integrated with large number of RC elements of very fine-grid thermal model significantly increases the simulation time. Moreover, different time scales of the thermal grid (\sim milliseconds) and transistor circuits (pico- to nanoseconds) cause simulation issues. To alleviate the above challenges, the thermal mode was regridded with fewer nodes. We defined an 81 element chip of size 9 mm \times 9 mm with a 3 mm \times 3 mm

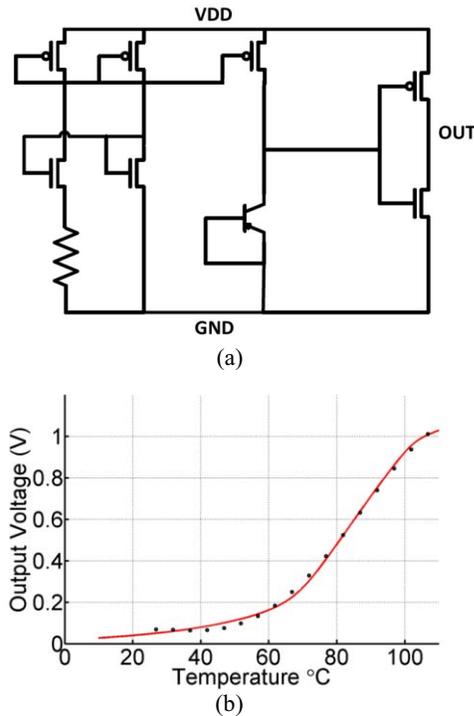


Fig. 5. (a) Temperature sensor circuit schematic. (b) Temperature sensor output characteristics and polynomial fit.

TEC in the center. The difference in accuracy of the resulting temperature profiles were verified to be within 2 °C. A power pulse with 10 W baseline power and a high power of 42.4 W was applied. The high-power pulse was applied at 100 ms and remained on until the end of the simulation. The total heat flux of the power pulse was 52.35 W/cm². The HTC used to model the system was set to 625 W/m²K, representing the low end of the cooling capabilities provided by commercial heat sink solutions.

A. Temperature Sensor Design and TEC Electrical Model

A temperature sensor was implemented with a constant current source going into a diode-connected Bipolar Junction Transistor and generating a known voltage at a given temperature [Fig. 5(a)]. Because the voltage measured across the diode only varies by about 1–2 mV/K and we are only interested in a small range of temperatures for controlling the TEC, we have added an amplifier to the output of the diode. This amplifier provides rail to rail output voltage within the high gain region falling between 60 °C and 100 °C. This will ensure that the sensor output will be close to ground when the chip is running in a low-power state and close to VDD at very high chip temperatures. The output characteristic of the temperature sensor is shown in Fig. 5(b). As we can see the sensor's high gain region is located between 60 °C and 100 °C. We fitted a fourth-order polynomial to the sensor output so that the temperature to voltage conversion could be done within our electrothermal cosimulation environment (in the cosimulation environment the temperature is represented by the voltage at the nodes of the distributed RC grid). The polynomial fit is also shown in Fig 5(b). The voltage of the silicon layer from

the RC thermal grid is an input for the polynomial source, which in turn converts the voltage between 0 and 1.2 V to provide input to the controllers.

B. Threshold-Based Controller

Fig. 6(a) shows a top-level schematic of the ThBC. The output voltage of the temperature sensor (represents the chip temperature), is compared with a reference representing a predefined target temperature. The comparator is implemented using an open-loop architecture with a folded cascode input pair followed by a common source stage and two levels of buffering to drive the current sourcing power transistor. The PFET input folded cascode comparator was chosen for better input range allowing the input voltage to go all the way down to ground. The power FET is implemented using a large on-chip transistor with low $R_{ds,ON}$ (50 mΩ) and proper current sinking capability. The current through the TEC will be set by the TEC supply voltage.

The ThBC was integrated with the full package thermal model to run full system simulations. The current through the power FET is fed as an input to the thermal TEC compact model and the TEC is turned ON when the comparator output is high. Fig. 6(b) shows the regulation of the silicon temperature (simulations with HTC = 625 W/m²K). When the generated heat is high enough that that the TEC cannot reduce the silicon temperature, the TEC remains ON but the temperature also continues to increase. It can be observed that at low TEC currents, the power pulse can be sustained for shorter times. Increasing the current initially helps to increase the time duration as shown. However, at higher current the Joule heating contribution is also higher. Consequently, increasing the current beyond a certain point actually reduces the overall extension period. Therefore, a careful choice of the TEC current is required to maximize the extension time. Note that once the temperature exceeds the threshold of the microprocessor, the DTM or throttling mechanism will be invoked to reduce the power dissipation itself.

C. Maximum Cooling-Based Controller

Fig. 7 shows a top-level schematic of the MCBC. The controller is based on a sample and hold (S/H) architecture with two S/H circuits sampling the temperature sensor. The S/H circuits are designed using transmission gate switches that are sampling the input to a 100-fF capacitor. At each time, the output of the first S/H circuit is the positive input of a clocked comparator. A time-shifted value ($t + \Delta$) of the temperature sensor [with programmable delay (Δ)] is sampled by a second S/H circuit, and the output is sent to the negative terminal of the comparator. Given this, the comparator should output a digital 1 if the more recent temperature $T(t)$ is lower than the previously sampled $T(t - \Delta)$. This means that the TEC will remain on if the temperature is strictly decreasing. Once $T(t)$ exceeds $T(t - \Delta)$ the comparator will switch and output a digital 0 turning the TEC OFF. Since we do not want the controller to turn ON the TEC when the chip temperature is decreasing (during a low-power event where

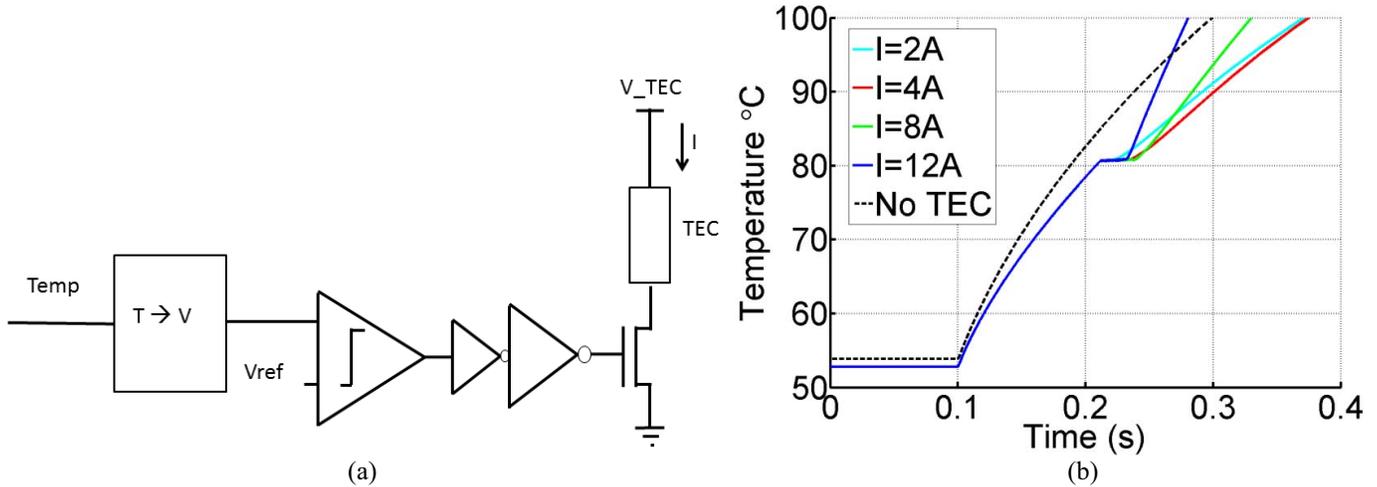


Fig. 6. ThBC (a) circuit schematic and (b) simulation results.

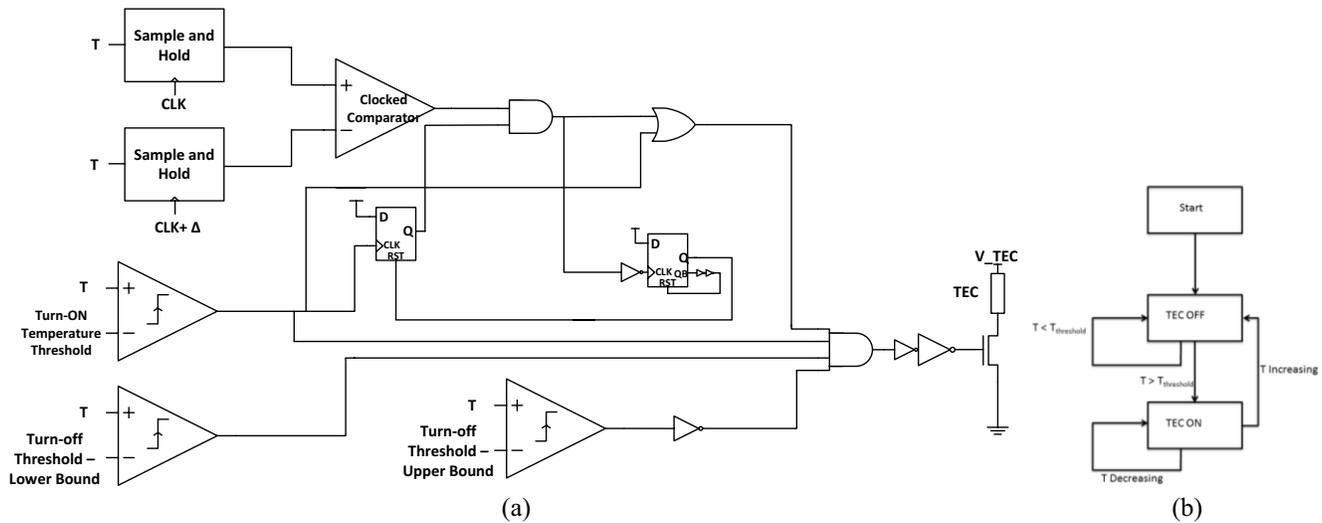


Fig. 7. MCBC (a) top-level architecture and (b) TEC state transition principle.

cooling is not required), we would like the MCBC to turn the TEC ON only beyond a certain temperature. We have therefore added a threshold temperature detector that will only turn the TEC ON once the temperature reaches a specified threshold using a positive edge detector circuit. This will ensure that the TEC is turned ON and the differential control signal from the S/H circuits will be used to keep the TEC ON until the maximum cooling is reached. Once the maximum cooling is reached, a negative edge detector will detect the differential control signal and reset the previously described positive edge detector. This will keep the TEC OFF until the threshold is once again reached. Fig. 7(b) shows a flow diagram to explain the operating principle of the MCBC. This process will continue until the TEC cannot provide any more cooling and the processor will have to be throttled by DTM techniques.

We integrated the MCBC controller within our thermal package and simulated the response using the power pulse used in the ThBC simulations. As shown in Fig. 8, the temperature starts to increase initially until the threshold temperature is reached and the TEC turns on (simulations with

$HTC = 625 \text{ W/m}^2\text{K}$). The TEC immediately begins cooling and the differential controller continues to keep the TEC turned ON as the temperature is decreasing. Once the temperature reaches the minimum point, the differential controller is turned OFF and resets the controller to monitor the temperature until it again reaches the threshold. The TEC again turns ON and the differential control takes over until the temperature is strictly decreasing. As expected the cooling of successive dips becomes lower as the Peltier cooling of the TEC is reduced due to the Joule heating. Eventually the TEC cannot provide cooling when turned ON at the threshold temperature, leaving the chip temperature to continue to increase until a given DTM technique is invoked to minimize the power dissipation. It can be observed that the higher levels of current provide more initial cooling but the larger Joule heating causes the cooling dips to have shorter duration. It can be observed that MCBC reduces the number of ON/OFF transitions of the TEC.

If the temperature of the chip goes below the specified threshold, the TEC will always turn OFF (irrespective of whether a local minimum has been reached) using a

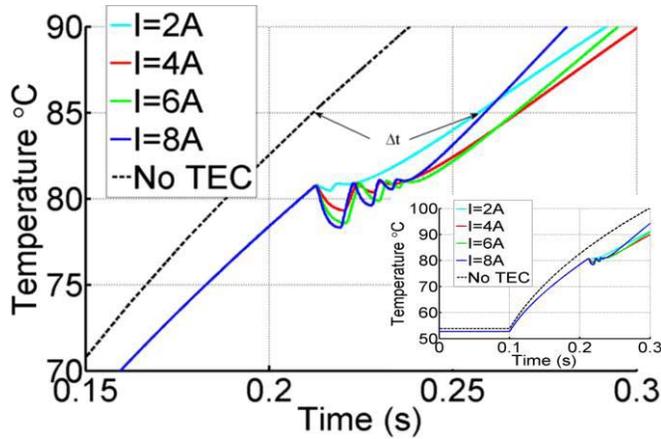


Fig. 8. MCBC. Transient temperature variation for varying levels of TEC current. Inset: complete transient response showing that WITH TEC the temperature is lower than the NO TEC case even when the TEC is off.

lower-bound comparator shown in Fig. 7(a). This helps to prevent unnecessary energy dissipation in the TEC in the case that a high-power pulse, that turned on the TEC and triggered the differential controller, disappears within a relatively short interval allowing the chip to cool naturally. The temperature response of the system for such a test case (i.e., a short duration high-power event that triggers the hysteretic control) is shown in Fig. 9. The test case considers a high-power event until 45 ms when the chip power goes to zero. As we can see, the chip temperature is increasing and the MCBC controller turns the TEC ON. Shortly after the power goes to zero and the temperature reduces because of natural cooling. The lower-bound threshold for the TEC is set at ~ 67 °C for this simulation and it can be observed that the TEC turns OFF at about 55 ms. The temperature has a slight increase around this point as the Peltier current source has been turned OFF and the heat cannot flow through the TEC increasing the silicon temperature. Beyond 70 ms, the temperature begins to decrease and eventually settles to a low steady-state value.

Once the TEC has exhausted, its cooling ability and the temperature system invokes the DTM, the TEC should be turned OFF to save energy and allow the system to cool naturally under DTM. This can be accomplished using an additional comparator in both the ThBC and MCBC.

VI. ANALYSIS AND DISCUSSIONS

A. Controller Comparison and Overhead Analysis

The overall characteristics of the two controllers are summarized in Table I. The simulation results show that with the proper choice of TEC current, both the controllers can achieve ~ 50 – 60 ms of time extension, which is quite significant at the microprocessor time scale. This time can be used to finish a workload without throttling and/or allocation to a different core in the chip. As explained earlier, increasing the TEC current initially increases the time extension due to more efficient transient cooling, but beyond a certain point, due to Joule Heating, the extension reduces. We further observe that the ThBC provides slightly longer extension times; about 1 ms greater on average for a given TEC current. The tradeoff

TABLE I
CONTROLLER CHARACTERISTICS WITH VARYING TEC CURRENT

| ThBC Results | | | | | |
|--------------|-----------------|------------------|-------------------|-----------------|-----------------------|
| TEC Current | Δt (ms) | # of Transitions | Average Temp (°C) | TEC Energy (mJ) | Power FET Energy (mJ) |
| 1 | 35.6 | 1 | 82.57 | 3.98 | 1.76 |
| 2 | 45.2 | 7 | 82.24 | 19.57 | 8.66 |
| 3 | 52.2 | 15 | 82.04 | 48.41 | 21.42 |
| 4 | 56.2 | 21 | 81.90 | 88.23 | 39.04 |
| 5 | 57.5 | 25 | 81.80 | 134.75 | 59.62 |
| 6 | 56.4 | 29 | 81.74 | 180.62 | 79.92 |
| 7 | 53.5 | 30 | 81.67 | 223.14 | 98.735 |
| 8 | 49.4 | 30 | 81.63 | 252.4 | 111.68 |
| 12 | 31 | 24 | 81.43 | 253.84 | 112.32 |
| MCBC Results | | | | | |
| TEC Current | Δt (ms) | # of Transitions | Average Temp (°C) | TEC Energy (mJ) | Power FET Energy (mJ) |
| 1 | 35.6 | 1 | 82.57 | 3.96 | 1.755 |
| 2 | 45.2 | 3 | 82.24 | 19.57 | 8.66 |
| 3 | 52.1 | 5 | 81.96 | 49.22 | 21.78 |
| 4 | 55.9 | 5 | 81.72 | 92.21 | 40.8 |
| 5 | 56.7 | 5 | 81.51 | 145.21 | 64.25 |
| 6 | 55.1 | 7 | 81.41 | 199.33 | 88.2 |
| 7 | 51.6 | 7 | 81.32 | 252.49 | 111.72 |
| 8 | 46.9 | 7 | 81.30 | 296.51 | 131.2 |
| 12 | 25.9 | 5 | 81.24 | 361.24 | 159.84 |

TABLE II
ENERGY ANALYSIS OF THE CONTROLLERS

| Controller Energy Analysis | | |
|----------------------------|------------------------|------------------------|
| TEC Current (A) | ThBC Energy (μ J) | MCBC Energy (μ J) |
| 2 | 0.550 | 1.978 |
| 5 | 0.526 | 1.898 |
| 8 | 0.528 | 1.980 |
| 12 | 0.546 | 2.102 |

is that the MCBC provides a lower number of transitions, three to seven compared with the ThBC, which has about 7–30 transitions. The reduced number of transitions can improve the reliability of the TEC, as a fewer transitions could extend the TEC lifetime [25]. The MCBC also results in a lower average temperature during the power pulse, about 0.3 °C on average when compared at same current levels.

Next we characterize the energy overhead of each controller. To accurately estimate the overhead, a piecewise linear curve of the temperature profile of the chip as shown in Figs. 6 and 8 are applied to the appropriate controller. The energy overheads originate from three main sources: 1) the operating power of the controller including the switching energy dissipation while driving the gate capacitance of the power FET; 2) the power loss in the TEC ($I^2 R_{TEC}$); and 3) the loss due to the finite on resistance of the power FET during on period ($I^2 R_{DS-ON}$).

The varying levels of switching activity within the controller circuits do not contribute much to the energy dissipated in

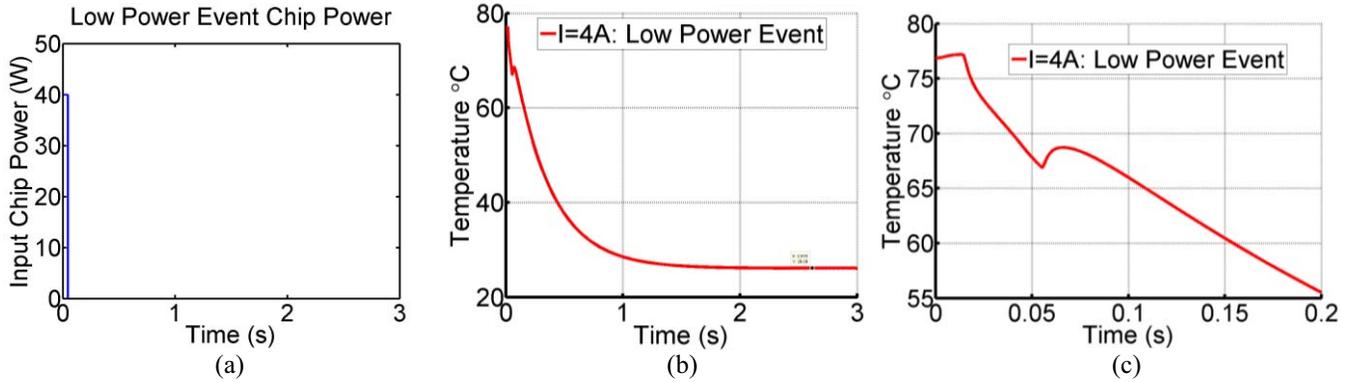


Fig. 9. McBC with low-power event. (a) Applied power pattern. (b) Observed temperature pattern. (c) Zoomed-in view near 100 ms to show the TEC operation. The power turns off at 45 ms and the TEC shortly after at ~ 5 ms.

the controller as most of the energy is in the analog block's biasing currents. Since the MCBC has more analog control blocks (mainly the comparators), the biasing (static) energy is higher for the MCBC. A higher number of transitions in the TEC tend to add additional switching energy due to the gate capacitance of the power FET and the output capacitance at the intermediate node between TEC and FET, but the switching energy has negligible contributions to the overall controller energy in both the ThBC and MCBC. However, as shown in Table II, the controllers' energy is almost insignificant when compared with the TEC energy.

The power dissipation of the TEC increases significantly with increasing levels of TEC current. This suggests the choice of the TEC current is a tradeoff between the time extension and energy overhead associated with cooling. The analysis of the energy overhead as a function of the control principle and TEC current is an interesting problem. The maximum energy overhead of the TEC occurs when the TEC is always ON and continuously consumes current. The ON power of the TEC is defined as $P_{\text{TEC}} = I_{\text{TEC}}^2(R_{\text{TEC}} + R_{\text{FET}})$. The maximum energy overhead can be computed as: $OV_{\text{MAX}} = P_{\text{TEC}}/P_{\text{chip}}$ and is summarized in Table III. The equivalent resistance of the TEC is ~ 113 m Ω [1]. The power FET was designed for 50 m Ω ON resistance in a 130-nm CMOS process and had an area of 600 $\mu\text{m} \times 600$ μm in layout, about 5% of the total TEC area. For example, the peak chip power dissipation in this analysis was 42.4 W, for 4-A current the maximum energy (or power) overhead of the TEC will therefore be 6.2%.

A more accurate analysis of the energy overhead needs to consider the fact that the TEC may not be always ON and it goes through ON and OFF cycles depending on the control principle. Assume a power pulse of duration T , which results in a total chip energy $E_{\text{chip}}(T) = P_{\text{chip}}T$. The energy consumed by the TEC for the same time duration of T is given by $E_{\text{TEC}}(T) = E_{\Delta T} + I_{\text{TEC}}^2(R_{\text{TEC}} + R_{\text{FET}})(T - \Delta T)$; where $E_{\Delta T}$ is the energy dissipated during the extension time of ΔT . The second component of the preceding equation defines the energy dissipation of the ON TEC beyond the extension period. The energy overhead for a duration T is defined as $OV(T) = E_{\text{TEC}}(T)/E_{\text{chip}}(T)$. Table III summarizes the analysis of the overhead considering a 100-ms power pulse. The TEC current and the control principles impact both ΔT

and $E_{\Delta T}$ (as illustrated in Table I) and hence, modulate the energy overhead: 1) the extension time ΔT depends on the current and control principles and 2) the energy dissipation during the extension time ($E_{\Delta T}$) depends on how long the TEC (and FET) remains ON in this period which in turn depends on the TEC current and the control principle. As explained earlier, ΔT initially increases with TEC current but start to reduce beyond a certain point. However, due to the quadratic relation between the TEC/FET energy and I_{TEC} , we observe that the overall energy overhead is always increasing with increasing TEC current (Table III). During the extension period the MCBC keeps the TEC on for a longer period and hence, results in higher energy dissipation in the TEC and FET compared with the ThBC (Table I). Further, the MCBC also have a marginally lower extension time compared with ThBC. Therefore, we observe that for a given TEC current, MCBC consumes marginally more energy than the ThBC even with less number of transitions.

In summary, both the control principles have a similar tradeoff between TEC current and time extension. The choice between the two control principles depends on the marginally higher extension time and lower overhead for ThBC versus the reduced number of transition and marginally lower average temperature in MCBC.

B. Effect of HTC on TEC Performance

Fig. 10 shows the effect of varying HTC from the chip on the effectiveness of the TEC-assisted cooling. Heat sink solutions for microprocessors have different sizes and fluid flow rates, which account for changes in the effective amount of heat that can be removed from the chip (external cooling). As observed from the figure, the initial steady-state temperature is higher for the lower HTC case. When the power pulse is applied, the temperature increases at a faster rate with a lower HTC and the threshold temperature is reached earlier. Moreover, with a higher HTC, the controller is able to sustain the threshold temperature for a longer period and hence provide a longer time extension for both ThBC and MCBC. Further, in the case of MCBC, once the cooling begins we observe deeper dips in the temperature profile with higher HTC. Therefore, we expect a lower average temperature

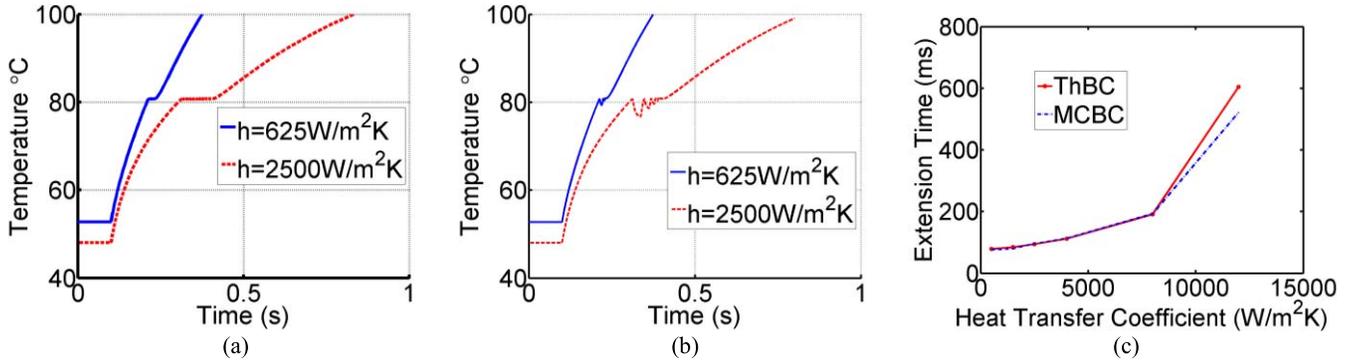


Fig. 10. Effect of HTC on the controller operation. (a) Effect of HTC on ThBC. (b) Effect of HTC on MCBC. (c) Effect of HTC on ThBC and MCBC time extension.

TABLE III
ENERGY OVERHEAD FOR TEC-ASSISTED COOLING

| TEC Current | TEC Energy Overhead in % [$P_{\text{chip}}=42.4\text{W}$] | | |
|-------------|--|--|------|
| | Maximum Overhead (OV_{MAX}) | Overhead with 100ms Power Pulse of 42.4W (OV(100ms)) | |
| | | ThBC | MCBC |
| 1 | 0.4 | 0.4 | 0.4 |
| 2 | 1.5 | 1.5 | 1.5 |
| 3 | 3.5 | 3.3 | 3.3 |
| 4 | 6.2 | 5.7 | 5.8 |
| 5 | 9.6 | 8.7 | 9.1 |
| 6 | 13.8 | 12.2 | 13.0 |
| 7 | 18.8 | 16.4 | 17.7 |
| 8 | 24.6 | 21.0 | 23.2 |
| 12 | 55.4 | 46.8 | 53.3 |

with MCBC at higher HTC. Fig. 10(c) shows that a higher HTC results in a larger time extension for both the ThBC and MCBC. This proves that the TEC is effective across all external cooling solutions, but is benefited from having a better external cooling solution.

C. Simulation Considering Architecture and Workload

In this section, we verify the TEC-assisted cooling considering processor workload-driven power estimates. The power trace was generated via architectural simulations to reflect the characteristics of executed workloads and microarchitecture. The SPEC2006 benchmark suite was executed with a detailed cycle-level x86 timing simulator, Zesto [26]. Zesto was configured to model a four-issue out-of-order pipeline, whose configuration is summarized in Fig. 11, and it was used to generate access counts of architectural components. The access counts indicate how the workload exercises different architectural components. In conjunction with Zesto, McPAT [27] was used to estimate the energy dissipation of architectural components. Dynamic energy is calculated by multiplying access counts with estimated per-access energy, and the total power is the

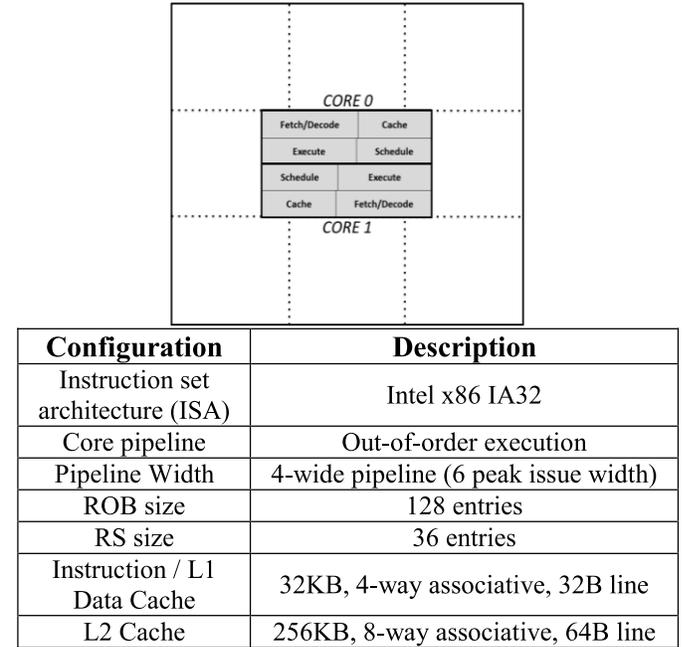


Fig. 11. Microarchitectural parameters and floorplan for the workload-driven simulation of TEC-assisted cooling.

sum of dynamic and leakage powers. A related work [28] used Zesto and McPAT with SPEC2006 benchmarks to validate the accuracy against Intel cores. The die floor plan, shown in Fig. 11, was made based on the area estimation provided by McPAT. The floor plan shows two cores underneath a $3\text{ mm} \times 3\text{ mm}$ TEC centered on a $9\text{ mm} \times 9\text{ mm}$ chip. Each core is partitioned into blocks by pipeline stages and cache. This is then converted to a grid using the exact sizes of each block and appropriate floor plan, and inserted under the TEC area. We have added 10 W background power elsewhere in the chip and ran the same simulation. The benchmark we used was sjeng (a relatively high-power workload) and it was simulated on a 1.2-V-OOO core implemented in a predictive 16-nm technology. The surface plot in Fig. 12(a) shows the power density (W/cm^2) at a time instant ($t = 100\text{ ms}$) across all elements (each element has a size of $1\text{ mm} \times 1\text{ mm}$) in the chip. It can be observed that the workload creates a hot spot in the cores. Fig. 12(b) shows the input transient

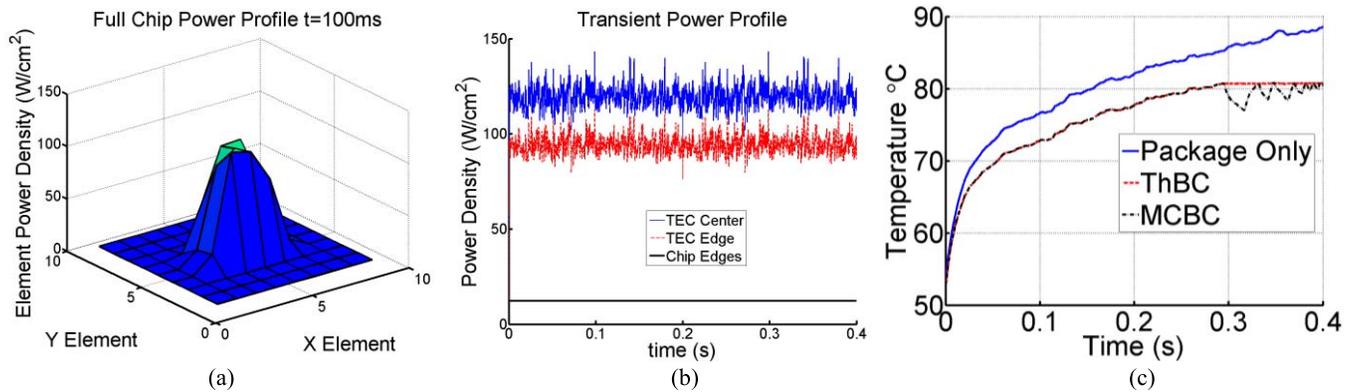


Fig. 12. Analysis of TEC-assisted cooling with a processor workload. (a) Full-chip power density pattern at $t = 100$ ms. (b) Time domain power density variation across sections of the TEC and background elements. (c) Transient temperature variation for the package, and the ThBC and MCBC at the TEC center. The workload is applied to the cores at the center of the chip (below the TEC) to demonstrate the nonuniform temperature density.

power variation across the center and edge of the TEC, as well as the chip edges where background power was applied. Fig. 12(c) shows that the TEC-assisted cooling allows us to maintain the hot spot temperature (the maximum temperature of the chip) below the threshold for a longer time. The above analysis validates that the proposed control principle works with a realistic processor workload.

VII. CONCLUSION

In this paper, we have studied the prospect of on-demand cooling with superlattice thin-film TECs integrated in a chip and package. We have demonstrated on-chip controllers for temperature-dependent dynamic activation/deactivation of TECs to provide on-demand cooling. The electrothermal analysis was performed integrating the transistor-level models of the control circuits, designed in 130-nm CMOS, with full-system thermal compact model of chip, package, and embedded TEC. The coanalysis shows that TEC-assisted transient cooling allows a processor to sustain a high-power pulse for a longer period without violation of the thermal threshold. This can significantly reduce the thermal events in processors and help improve thermally limited system performance, which will become critical in future generation systems. The possible performance gains of integrating TECs within a microprocessor package suggest the need for future work on this topic on designing more efficient controllers as well as on innovative approaches to exploit TEC-assisted cooling through microarchitecture-driven DTM approaches. The potential advantages of integration of TEC scan also inspire investigations in chip-package codesign.

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